IN THE CLAIMS:

Claims 1-9. (Cancelled)

10. (Currently amended) A read-only memory system where read-only data is stored in combinatorial logic, said system comprising:

at least one binary logic function device adapted to receive two binary address bits and to generate a plurality of binary values from said two address bits and a plurality of logic functions, said read-only data including at least one of said plurality of binary values.

11. (Original) The read-only memory system of Claim 10, further comprising at least one multiplexer adapted to receive at least one of said plurality of binary values, said read-only data being provided from an output of at least one of said at least one multiplexer.

12. (Original) The read-only memory system of Claim 11, wherein said at least one multiplexer is adapted to select a subset of said at least one of said plurality of binary values based upon at least one address bit, said at least one address bit being separate and distinct from said two address bits.

13. (Original) The read-only memory system of Claim 10, wherein said plurality of logic functions are selected from a list of logic functions consisting of AND, OR, XOR, NOT, NAND, NOR, and XNOR.

14. (Original) The read-only memory system of Claim 11, wherein said plurality of logic functions are selected from a list of logic functions consisting of AND, OR, XOR, NOT, NAND, NOR, and XNOR.

15. (Original) The read-only memory system of Claim 12, wherein said plurality of logic functions are selected from a list of logic functions consisting of AND, OR, XOR, NOT, NAND, NOR, and XNOR.

16. (Original) The read-only memory system of Claim 12, wherein at least one of said at least one multiplexer is selected from a list of multiplexers consisting of 2:1, 4:1, 8:1, and 16:1 multiplexers.

17. (Original) The read-only memory system of Claim 11, further comprising at least one decoder for decoding said at least one address bit.

18. (Original) The read-only memory system of Claim 12, further comprising at least one decoder for decoding said at least one address bit.

19. (Currently amended) A read-only memory system where read-only data is stored in combinatorial logic, said system comprising:

at least one binary logic function device adapted to receive two binary address bits and to generate a plurality of binary values from said two address bits and a plurality of logic functions;

at least one multiplexer adapted to receive at least one of said plurality of binary values, said at least one multiplexer being adapted to select a subset of said at least one of said plurality of binary values based upon at least one address bit, said at least one address bit being separate and distinct from said two address bits;

at least one decoder for decoding said at least one address bit; and

~~The read-only memory system of Claim 18, further comprising~~ at least one stage two multiplexer, where the output of said at least one multiplexer is provided to said at least one stage two multiplexer, the output of said at least one stage two multiplexer being said read-only data.

20. (Currently amended) A read-only memory system where read-only data is stored in combinatorial logic, said system comprising:

at least one binary logic function device adapted to receive two binary address bits and to generate a plurality of binary values from said two address bits and a plurality of logic functions;

at least one multiplexer adapted to receive at least one of said plurality of binary values;

at least one decoder for decoding said at least one address bit; and

~~The read-only memory system of Claim 17, further comprising~~ at least one stage two multiplexer, where the output of said at least one multiplexer is provided to said at least one stage two multiplexer, the output of said at least one stage two multiplexer being said read-only data.